REMARKS

The title, specification, abstract and claims have been amended in view of the Office action In view of the remarks which follow, the claims and application as a whole are believed to be in condition for allowance.

Restriction/Election

Referring to section 1 of the Detailed Action claims 12-20 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to non-elected inventions, based on the allegation that there is no allowable generic or linking claim have been canceled without prejudice.

Claim Objections

In part 4 of the Detailed Action objections were made to Claims 1 and 10 because of the reasons stated as follows:

"In claim 1, line 5, replace a term 'form' by - - forming - -,"

"line 8, 'remove' by - - removing --,"

"lines 9-10, 'deposit' by -- depositing --."

"In claim 10, lines 9-12 'after forming word lines and gate electrodes in the arry [sic] region and support region forming sidewall spacers on sidewalls thereof' is indefinite. Correction is required."

The required changes have been made.

Claim Rejections - 35 U.S.C. § 102

In part 5 of the Detailed Action claims 1 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by Huang (U.S. Patent No. 6,074,908) for the reasons as follows:

"Regarding claim 1, Huang discloses a method of forming integrated circuit device including at least one semiconductor memory array region and logic circuits including a support region including the steps as follows:

"form a thick deposit of polysilicon (16, Fig. 1) in both the array region (M, Fig. I) where word lines are located and where the support region (L, Fig. 1) where the logic circuits are located;

"then removing the thick layer of polysilicon (16, Fig. 1) only in the array region (M, Fig. 2)

"then depositing a thin layer of polysilicon (25, Fig. 3) in both the array region and the support region;

"then depositing a metallic conductor (26, Fig. 3) coating including at least an elemental metal layer portion over the thin layer of polysilicon (25, Fig. 3); and

"then forming word lines and gate electrodes in the array region and support region respectively. (Fig. 8)."

"Regarding claim 9, Huang discloses a capping silicon nitride layer (30, Fig. 3 and col. 5, lines 8-9) is formed over the metal layer before forming word lines and gate electrodes in the array region (M, Fig. 3) and support region (L, Fig. 3)."

Claim 1 has been amended to add limitations which are believed to render claim 1 and claim 9 which is dependent thereon patentable in view of Huang. In particular, the amended claim 1 states "forming word lines in said array region from said thin polysilicon layer and forming gate electrodes in said support region from said thick polysilicon layer and said thin polysilicon layer thereabove." Huang fails to teach that critical step in that there is no teaching that the first polysilicon layer 16 and the second polysilicon layer 25 of Huang are present in the gate electrode of either the logic L or the DRAM region M of the device of FIGS. 7-9 of Huang since Huang removes the first polysilicon layer 16 from the region M in FIG. 2 (Col. 4, lines 51-57) and Huang removes the second polysilicon layer 25 from the device in FIG. 7 (Col. 5, lines 59-67). Thus the steps of amended claim 1 are not suggested by Huang and since Huang was not attempting to solve the problems described in paragraphs [0020] to [0026]; nor does Huang suggest the solution described in paragraph [0027] of the present application, all of which paragraphs are incorporated herein by reference. Moreover, Huang teaches that the first polysilicon layer 16, Fig. 1 has a thickness "between about 1,000Å and 1,500Å" (Col. 4, lines 44-46) and that the second polysilicon layer 25, Fig. 3 has a thickness "between about 1,000Å and 1,500Å" (Col. 4, lines 64-67). In other words there is no teaching that the second polysilicon layer 25 is thinner than the first polysilicon layer 16, but it appears that they are equal in thickness.

Claim Rejections - 35 USC § 103

In part 6 of the Detailed Action under 35 U.S.C. 103(a) claims 4 and 8 were rejected as being unpatentable over Huang in view of Tseng (U.S. Patent No. 5,843,821) for the reasons as follows:

"Huang discloses all the features of the claimed invention as discussed above, but does not disclose the thin layer of polysilicon comprises amorphous silicon, wherein a gate oxide layer is formed over the device after formation of the sacrificial polysilicon layer."

"Tseng, however, discloses the thin layer of polysilicon comprises amorphous silicon, wherein a gate oxide layer (36A, Fig. 3) is formed over the device after formation of the sacrificial polysilicon layer (36, Fig. 2) [col. 5, lines 56]."

"It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above discussed teaching of Huang as taught by Tseng for a purpose of improving self-aligned node contact with smaller size."

Claim 1 upon which claims 4 and 8 are dependent has been amended to add limitations which are believed render claim 1 and claims 4, 8, and 9 patentable in view of Huang and Tseng. One reason is that there is no teaching that the first polysilicon layer 16 and the second polysilicon layer 25 are present in the gate electrode of either the logic L or the DRAM region M of the device of FIGS. 7-9 of Huang since Huang removes the first polysilicon layer 16 from the region M in FIG. 2 (Col. 4, lines 51-57) and Huang removes the second polysilicon layer 25 from the device in FIG. 7 (Col. 5, lines 59-67). Thus the steps of amended claim 1 are not suggested by Huang.

Moreover, Huang teaches that the first polysilicon layer 16, Fig. 1 has a range of thicknesses "between about 1,000Å and 1,500Å" (Col. 4, lines 44-46) and that the second polysilicon layer 25, Fig. 3 has an equal range of thicknesses "between about 1,000Å and 1,500Å" (Col. 4, lines 64-67). In other words there is no teaching that the second polysilicon layer 25 is thinner than the first polysilicon layer 16. In fact they may be equal or not.

As to Tseng with regard to claims 4 and 8, Tseng shows a thin polysilicon or amorphous silicon layer 36 which is later converted to a polyoxide layer 36A which is located several layers above the structure of gate electrode 16, which layers do not relate to formation of the structure of the gate electrode. Tseng also shows but does not describe what appears to be a conductor formed over a FOX region to the right of the gate electrode 16. The thin polysilicon or amorphous silicon layer 36 is formed above an oxidation barrier layer 34 which overlies a first conductive layer 30 formed over a first insulating layer 28 which covers the gate electrode stack including the gate electrode 16, which relates to a different process and a different resultant structure from what is claimed herein. Thus Tseng is not believe to be relevant to the

subject matter of the amended claims, since the layers 36/36A are not related to the same process or the same structure produced by the process of the amended claims. Huang and Tseng were not attempting to solve the problems described in paragraphs [0020] to [0026] of the instant application; nor do Huang and Tseng suggest the solution described in paragraph [0027] of the instant application, all of which paragraphs which are incorporated herein by reference.

In part 7 of the Detailed Action under 35 U. S. C. 103(a) claim 10 was rejected as being unpatentable over Huang in view of Applicant's Figs. 1-2 for the reasons as follows:

> "Huang discloses all the features of the claimed invention as discussed above, but does not disclose forming the integrated circuit device on a semiconductor substrate with a polysilicon stud is in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of the trench and an Array Top Oxide (ATO) layer formed above the substrate aside from the polysilicon stud; and after forming word lines and gate electrodes in the array region and support region; and forming sidewall spacers on sidewalls thereof."
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> "Applicant's Figs. 1-2 however, discloses forming the integrated circuit device on a semiconductor substrate with a polysilicon stud is in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of the trench and an Array Top Oxide (ATO) layer formed above the substrate aside from the polysilicon stud; and after forming word lines and gate electrodes in the array region and support region; and forming sidewall spacers on sidewalls thereof."
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> "It would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the above discussed teaching of Huang as taught by Applicant's Prior Arts for a purpose of improving a process of forming integrated circuit device."

Claim 1 upon which claims 10 is dependent has been amended to add limitations which are believed render claim 1 and claim 10 patentable in view of Huang and Applicant's Figs. 1-2 for the reasons stated above which are incorporated here by reference.

Allowable Subject Matter

In part 8 of the Detailed Action it was indicated that claims 2-3, 5- 7 and 11 contained allowable subject matte; but that there was an objection that claims 2-3, 5- 7 and 11 were dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Claim 2 has been rewritten into independent form in accordance with the above statement, so claim 2 as well as claims 3 and 7 which are dependent thereon are believed to be allowable because claim 2 has complied with the above conditions. The remaining claims indicated to be allowable are dependent upon claim 1 which is believed to be allowable as explained above.

New claims 21-29 are believed to be patentable for the reasons stated above.

In summary, the pending claims are now believed to be patentable over the cited prior art.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, please charge such fees to Deposit Account No. 09-0458.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,

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